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VLSIIMPLEMENTATIONOFKOGGE-STONEADDERFORLOW-POWERAPPLICATIONS

By

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ABSTRACT

The adder is a vital part of the central processing unit (CPU), the main processing unit of any device that can performcomputational operations. These are used in the digital components that are mostly used in the design of integratedcircuits. Recent decades have seen a sharp rise in demand for mobile electronics, which has increased the need forhighly efficient VLSI structures. All operations must be computed using low-power, space-efficient designs that runfaster.TheKogge-Stoneadder(KSA)isanextensionofthecarrylook-aheadadderusedforperformingfastadditioninhigh-performancecomputingsystems.Thelatency,space,andenergyusedbytheKogge-stoneadderafterdevelopment and implementation in Xilinx Vivado using Verilog are compared in this study to those of the RCA andCLA. The Kogge Stone adders (KSA) results show a decrease in power consumption as well as improvements in highspeed and area compaction when compared to the RCAand CLA.

Keywords:*Adder,Carrylook-aheadadder(CLA),Kogge-StoneAdder(KSA),RippleCarryAdder(RCA).*

INTRODUCTION

TheALUservesasthemainbuildingblockfordigitalprocessors(DSP),microprocessors,microcontrollers,andotherdata-processingdevices.Adderisanessentialhardwareunitforthefollowingapplicationinmanyarithmeticoperations.Theoptimizationofspeedandreduction of power consumption has a significant impact onthe latency andoverall energy used by the microprocessorsbecause adders are the most crucial component in ALU. TheKogge-Stone adder uses a tree-like structure that extendsthecarry-lookaheadadderbyparallelizingthecomputationofthecarrysignalsforseveralbitpositions.Thecarrysignalsforadjacentbitpositionsarecomputedforeachstage of the tree using the carry signals from the previousstage. The final sum and carry signals are calculated usingthe output carry signals from the tree's final stage. TheKogge-Stone adder's main benefit is its capacity for quickadditionwithashortcriticalpathdelay.Theaddercancompute the carry signals for several bit positions at oncethankstotheparallelprocessingemployedinthetreestructure,whichshortenstheoverallprocessingtime.Because of this, high-performance computing systems thatneedquickarithmeticoperationsfrequentlyusetheKSA.The primary goal of this paper is to implement the KSA andcompare it with other adders like RCA and CLA. The aboveadders have been simulated and synthesized on the XilinxVivadoplatformandtheirparametersarecaptured.ThespecificationsoftheXilinxVivadosoftwareareArtix–7families,csg324PackagewithSpeedGradeof–1.Finally captured parameters like latency, area, and energy used bytheabove-mentioned adders are compared.

1. Literaturesurvey:

Penchalaiah and Kurnar investigated the Kogge-stone adder,a new PPA architecture. The results of the application of theproposed method are verified by comparing the Kogge-stoneadder with Carry skip adder in terms of size, latency, andspeed [1]. A general procedure used in digital circuits tosimplify the circuit and its operation is the addition of acertainnumberofbits.Selectinganadderwiththeappropriate characteristics is even more important for thecircuittofunctionproperly[2].DaphniandVijulaGraceexplained the design and analysis of many parallel prefixadders and compared their performance in terms of area,latency,andpowerusage.[3].High-speeddesignsfrequently employ the carry-lookahead adder (CLA) and itsvariants,suchastheparallelprefix(PPF)adder[4].Although adders are necessary, the kind used depends ontheprogramintermsofspeed,powerconsumption,andarea usage[5]. Circuit designers benefit greatly from theabilitytoreachfasterrateswithlesspowerdissipation.Minimizing the supply voltage is a simple method to reducethe energy consumption of the circuits because there is aquadratic relationship between the switching energy and thevoltage [7]. To increase energy and speed, the designer canuseseveraladderstructuralmodifications.Therearemany

adder families, and they all have various delays, energyneeds, and spatial requirements. There are several differenttypes of adders, including parallel prefix adders, ripple carryadders,carryincrementadders,carryskipadders,carryselectadders,andcarrylook-aheadadders(PPA)[8].

2. Backgroundinformation:

There have been recent events that have a considerableincrease in the need for high-performance computing, whichhas prompted the creation of cutting-edge processors andmemoryarchitectures.Theportabilityandbatterylifeofmobile devices is, however, frequently constrained by thehigher power consumption that results from this improvedperformance. The creation of low-power computing systemsthat can deliver excellent performance while using the leastamount of power is becoming more and more popular as asolutiontothisproblem.Theperformanceandpowerconsumption of adders, which are essential components ofdigitalcircuits,significantlyaffectsthoseoftheentiresystem. In this research, we want to construct KSA for low-power applications using very large-scale integration (VLSI)approaches. To reduce power consumption while retainingexcellent performance, we will optimize the KSA design. Toshow the benefits of KSA in terms of speed and powerconsumption, we will also compare the performance andpowerconsumptionofKSAwiththatofotherfrequentlyused adders, such as the carry-lookahead adder (CLA) andripple carry adder (RCA). The overall goal of this project is toshowhowwellKSAperformshigh-speedarithmeticoperations, which will help in the development of low-powercomputing systems. Mobile devices, embedded systems, andhigh-performance computer systems can all benefit from theproject's findings in terms of increased performance andpowereconomy.

METHODOLOGY

Adders:

(I) Ripple carry adder (RCA):

A ripple carry adder is a simple digitalcircuit that adds two binary values. The carry signal ripplesovereachstageofthecircuitwhiletheadditionisdone,giving the circuit its name [6]. Each full adder in the circuitinputs two bits from the input numbers and the carry signalfrom the preceding step, and the outputs are a sum and acarry. The sum bit is output as a component of the final sum,while the carry bit from each full adder is sent on as the carrysignalto the following stage.

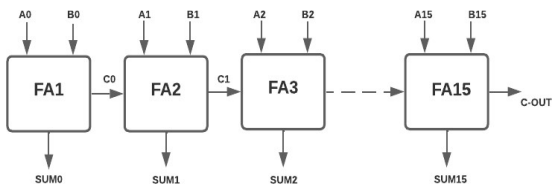


Fig-2.1.1:16-Bit Ripple carry adder

Intheabovediagram,A0toA15andB0toB15representthe

16-Bit binary numbers, while the output sum is denoted bySUM. The circuit uses sixteen full adders (FA) to compute thesum and carry bits for each bit position. The carry bits arepropagated from each stage to the next, resulting in a rippleeffectas the addition is performed.

(II) Carrylook-aheadadder(CLA):

Acarry-lookaheadadder(CLA)isaparalleladdercircuitadderthatcanreducethepropagationdelayofcarrysignals.Instead of waiting for the carry to propagate through theentire adder circuit, it uses a lookahead carry generator togenerate the carry signals for each bit in parallel. The CLAdivides the adder into bit groups, with each group having itslookaheadcarrygenerator.Eachgroup'scarrygeneratortakesthe input bits and generates the carry signals for that group.The carry generator determines the carry signals using a setofBooleanfunctionsbasedontheinputbits.Eachcarrygeneratorproducesasetofcarrysignalsforthatgroup,which are then combined with the previous group's carrysignals to produce the carry signals for the next group. Thisprocessis repeated until thefinal carry signal is produced.

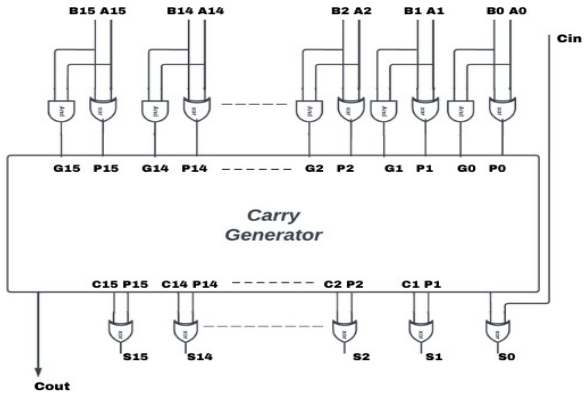


Fig-2.2.1: 16-BitCarrylook-aheadadder

In the above diagram, A (A0 to A15) and B (B0 to B15)representtheinputnumbers,whiletheoutputsumisdenoted by S (S0 to S15. The adder unit then takes in theinputnumbersandthecarrysignalsandperformstheaddition to generate the final sum.

The carry generator unit consists of a series of carrylookahead logic gates, which generate the carry signals foreach stage of the adder in parallel. By calculating the carrysignalsinparallel,theCLAcansignificantlyreducethepropagation delay compared to a ripple carry adder, resultinginfaster operation.

(III) Kogge-stoneadder(KSA):

The Kogge-Stone adder is a parallel adder that computes thesum of two binary numbers at high speed. It is similar to thecarry-lookahead adder, but it generates the carry signals inparallelusingatree-basedstructure,resultinginfasteroperation. The Kogge-Stone adder is made up of a series offull adders that are arranged in a tree-like structure. Each fulladder accepts two input bits and a carry bit and outputs asum bit and a carry bit. Each full adder's carry bit output isthen propagated up the tree to the next level, where it iscombined withthe carrybitsfrom theotherfull addersinthat

level to produce the next set of carry bits. The completefunctioningofKSAcanbeeasilycomprehendedbyanalyzingitin terms of the following three distinct parts:

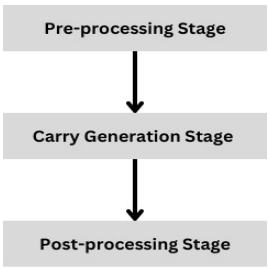


Fig-2.3.1: StagesofKogge-

stoneadder(i)Pre-processingStage:
This process includes calculating the propagate and generatecarry that corresponds to each pair of bits in A and B. Thelogicequations below provide these signals:
Propagate carry (Pi) = Ai XOR
BiGeneratecarry(Gi)= AiAND Bi

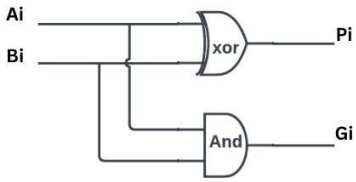


Fig-2.3.2: Logicdiagramofthepre-processingstage

(ii) CarryGenerationStage:
This block distinguishes KSA from other addersand is the force behind its superior performance. This stepincludes calculating the carries associated with each bit. Itemploysgroupppropagationandgeneratesintermediatesignals, which aregiven by thefollowing logicequations**:**

G= (Pi AND Gi*) +Gi P = (Pi AND Pi*)

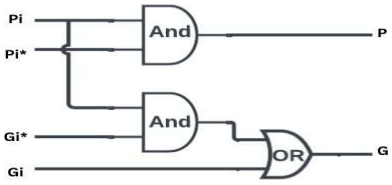


Fig-2.3.3: Logicdiagramofcarrygeneratorstage

(iii) Post-processingStage:
This is the final step, which is shared by all adders in thisfamily (carry look ahead). It involves the calculation of sumbits. The logic shown below is used to compute sum bits:

Ci=GiSi=P
iXORCi-1

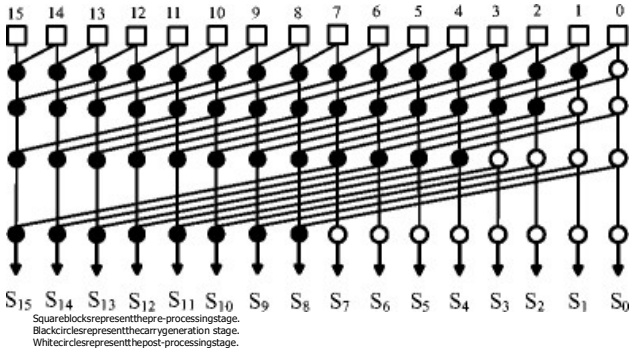


Fig-2.3.4: 16-Bit Kogge-stone adder

[9]RESULTS**:**

(I) Simulation outputs:

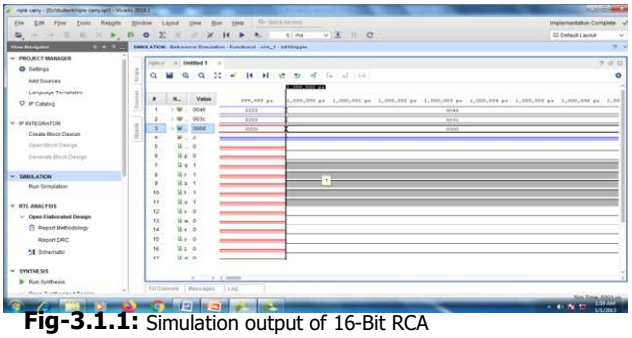


Fig-3.1.1: Simulation output of 16-Bit RCA

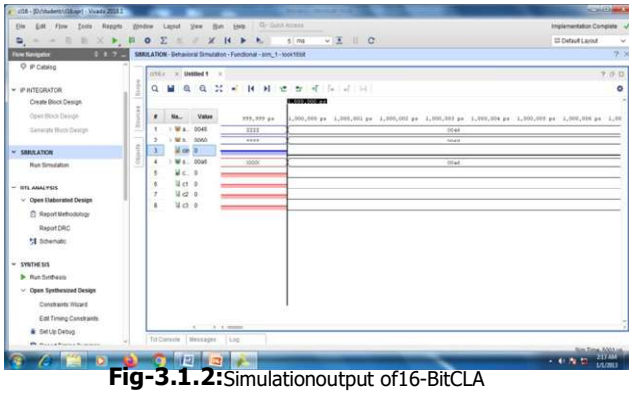


Fig-3.1.2: Simulationoutput of16-BitCLA

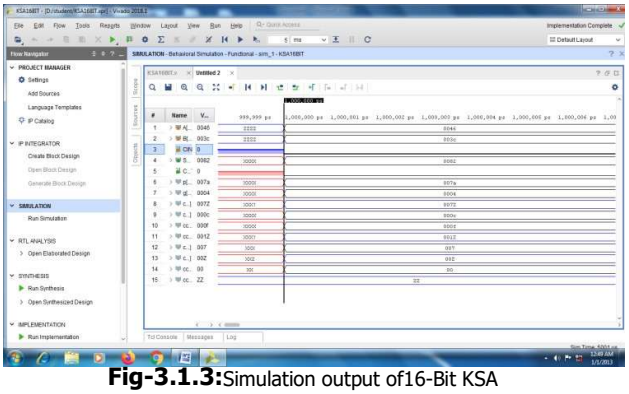


Fig-3.1.3: Simulation output of16-Bit KSA

(II) Poweroutputs:

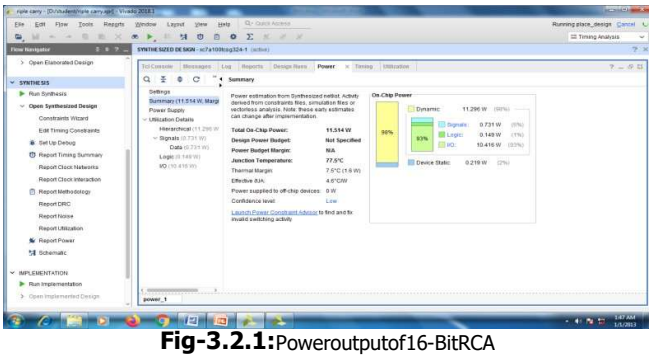


Fig-3.2.1: Poweroutputof16-BitRCA

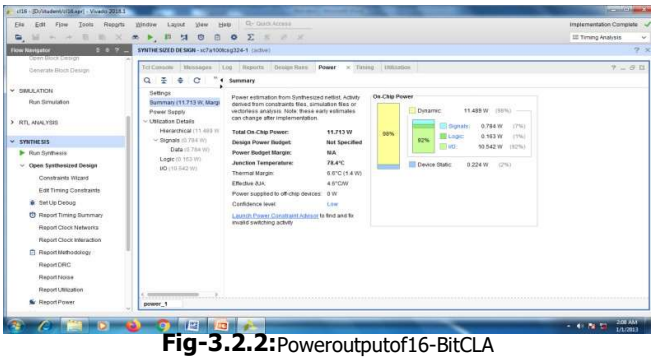


Fig-3.2.2: Poweroutputof16-BitCLA

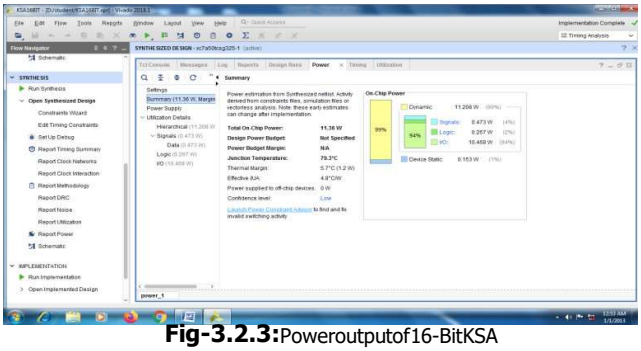
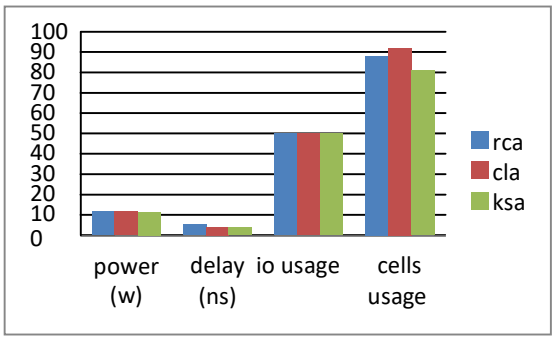


Fig-3.2.3: Poweroutputof16-BitKSA

COMPARATIVEANALYSISOFADDERS:

PARAMETERS	**RCA**	**CLA**	**KSA**
POWER	11.514w	11.713w	11.36w
Delay	5.26ns	4.12ns	3.77ns
IO (utilizationout of 210)	50	50	50
Cells (rtl schematic)	88	92	81

Table-1: ComparisonTable



Graph-1: ComparisonGraph

CONCLUSION:

In conclusion, the implementation of the KoggeStone adder for low-power applications is an effectiveapproachforreducingpowerconsumptionindigitalcircuits. Kogge Stone adder is a parallel prefix adder thathas a regular and scalable structure, which allows forefficient implementation and optimization. It is particularlywell-suitedforapplicationsthatrequirehigh-speedadditionoflargenumbers,suchasindigitalsignalprocessing,graphicsprocessing,andcryptography.

In summary, the Kogge Stone adder is a promising adderarchitectureforlow-powerapplications,withseveraladvantagesoverotheraddera rchitectures.Withcontinued research and development, it is likely to remainakeycomponentinthedesignoflow-powerdigitalcircuits.

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