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DelayReductioninThreeoperandbinaryadder

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Abstract— Today's world places a high value on a processor'sability to operate its arithmetic logic units (ALU).The delay inprocessingan outputisusedtogaugetheefficiencyoftheArithmetic Logic Units (ALU). Addition is the fundamentaloperational unit of all arithmetic logic units (ALUs). So, usingparallel prefix three operand binary adders, which are moreefficientthanotheraddersandthePropagatorgenerator,which has a great delay performance, we have presented anadditiontechniqueinthisstudy.Thesuggestedadderoutperforms the current three operand parallel prefix adder intermsofhardwareefficiency(1.1534)anddelayefficiency(1.07291).

I. INTRODUCTION

Making a high speed parallel prefix three operandbinary adder isthe major goalof this paper.Thethree-operandbinaryadderisthefundamentalfunctionalcomponent used in many cryptography and pseudo randombitgenerator(PRBG)techniques,aswellasotherapplications, to carry out modular arithmetic. (Carry SaveAdder),oftenknownasCS3A,isthemost popultechnique for performing three-operand addition. The mostcommonly used parallel prefix three-operand binary addersare Brent-Kung adder, Ladner Fischer adder, propagator-generatoradderarethemostcommonlyusedparallelalgorithms.

Hybrid adder is the name of the proposed adderalgorithmforanovel,high-speedthree-operandadder.Using Very High Speed Hardware Description Language(VHDL), the proposed adder was created. It is simulatedwith the help of Altera Quarts II 8.0 which is an ElectronicDesign Automation tool. Thus the synthetization is verifiedfor the performance in Altera ACEX1K:EP1K50TC0144-3.The results and the comparison have been discussed in theupcomingcontent.

II. WHATISTHREE OPERANDBINARYADDITION

The fundamental building block for carrying out allhigher level to lower level operations is the three operandbinary addition. (Han-carlson) adder is the fast and efficientmethodforaddingtwobinarynumbersinparallel.Theoperation of addition in Han Carlson adder is performedwith involvement of two individual two operand additions.Eventhoughthisadderalgorithmisconsideredtobeafastermethodinthreeoperandaddition.Itisinefficientforhigher bit rates as it is similar to that of an operating algorithm ofbasicripple-carryadder(RCA).Toovercometheabovementioned delay issues in the Han-Carlson adder variousthreeoperandbinaryadditionandsoon.
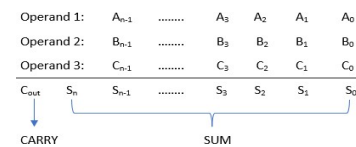

Fig 1.Modesofoperation

III. BASICELEMENTS OFPARALLELPREFIXADDER

A. Greycell

Agreycellisthefundamentalblockusedinparallel prefix addition logic. And it consist of a ANDand OR gate. It has one output and three inputs. It is areusable part that, by permitting many instantiations invarious designs, improves modularity and cuts down ondesigntime.Ingeneral,greycellsareacrucialcomponent of the VLSI design technique, allowing forthequickandefficientdevelopmentofintricateintegrated circuits.
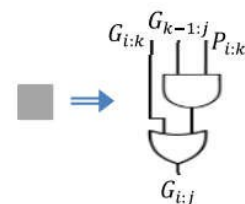
$$G_{i:j}=G_{i:k}(OR)P_{i:k}(AND)G_{k-1:j}$$

Fig 2(a). Greycell

B. Blackcell

Ablackcellisanotherfunctionalbuildingblockinparallel prefix addition logic. And it consist of two ANDgates and one OR gate. It is the combination of AND andOR gates. It has the pin configuration of four inputs and twooutputs.ItistheintegratingofgreycellwithaANDlogic.

InwhichtheoutputofAND logicispropagationindex($P_{i:j}$).Andtheoutputfromthegreycellisgenerator($G_{i:j}$).

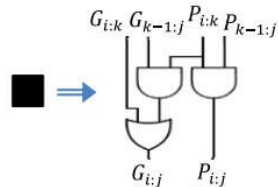$$G_{i:j}=G_{i:k}(OR)P_{i:k}(AND)G_{i:k-1:j}$$

$$P_{i:j}=P_{i:j}(AND)P_{k-1:j}$$

Fig 2(b).Blackcell

IV. PARALLEL PRIFIXADDER

The concept behind the prefix adder is parallel prefixcomputation,whichincludescreatingprefixsumsconcurrentlyforasetofinputdata.Theprefixaddercomputesthesumoftwobinaryvaluesinthecaseofaddition by first producing a collection of partial sums andthen merging them to yield the complete total. Prefix addersare superior to other types of adders in a number of ways,including quicker addition times and improved scalabilityforlargeroperands.Itisfrequentlyemployedinhigh-performancearithmeticcircuits,includingthoseinmicroprocessors, digital signal processors, and other digitalsystems. The Ladner Fischer Adder, the Brent-Kung Adder,and the Propagator Generator are a few examples of prefixadders.

A. LadnerFischerAdder

A quick way to add binary integers is to use the Ladner-Fischer adder, also referred to as the carry-skip adder. Thesystem blocks the integers and adds separately inside eachblock.Thecalculationofthecarrybitsbetweentheblocksisdone in parallel, which cuts down on processing time. Toavoidcarrybits,themethodusesblockadders,acarrygenerator, and a carry skip network. This method expeditesaddingbut necessitatesmoreintricate circuitry.
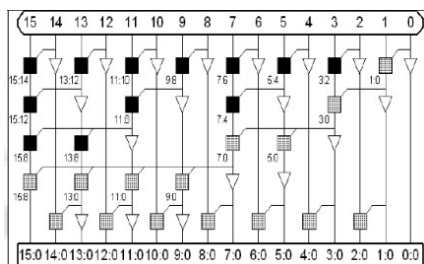

Fig3(a).Ladnerfischeradder

B. Brent-kungAdder.

Brent introduced Brent -Kung. Maximum logic depth isachieved by Brent-Kung adders, although they have fewinterconnectsandlittlespace.Createsumsforevenbitpositions first, then for odd bit locations. It determines theprefixforgroups,whichisthenusedtodeterminetheprefix

for an 8-bit group, which is then used for a group of 16-bitsand higher order words. The carry-in bits are then calculatedbytheaffixesbytrackingbackwardsateachlevel.Structured adders that resemble trees need 2log2n-1 stages.Black and grey cells are typically employed as buffers tolessenfan-out.Thisaddermaybecreatedfor23,24,and25-bitutilisingCMOSlogicandTransmissiongates.The16-bitBrent-Kung'sstructureisshowninthefollowingimage.
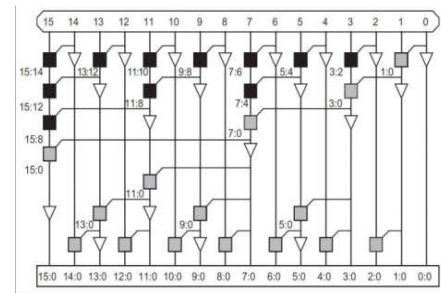

Fig3(b).Brent-Kungadder

C. PropagatorGenerator

The propagation generator adder produces the necessarycarry bits to finish the N-bit pair modulo-3 sums in parallelwhenusedwithamodulo-3N-bitoperandadder.Becauseofthelogicstructure'slog23Noperatinglevels,constantfan-inandfan-outdesignsarepossible,aswellasstaticprecharge/dischargeoperationsopposedtofixed-rateprecharge/discharge.Thenetworkcanalsobeusedasaconditional sum selection controller for a conditional sumadderina simplerform.
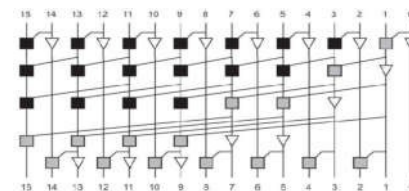

Fig 3(c).Propagation generator

V. PROPOSEDADDER

The proposed adder has the three operand parallel prefixadderintermsofoptimizinghardwareresourcesandimprovingthecomputationspeed.Additionally,theincorporationofdelayreductiontechniques,includingpropagationdelayoptimizationandgate-leveloptimizations,reduces the overall delay in the adder circuit. We proposedit hashybridadder.
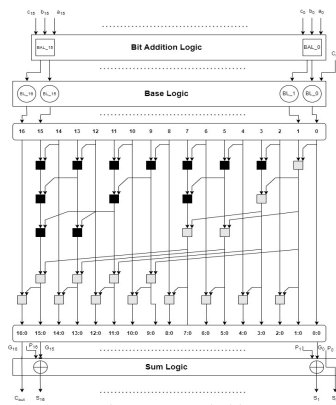
Fig4.Proposedadder

reducestheoveralldelayintheaddercircuit.Theseoptimizations enhancetheperformanceoftheadder,makingit suitable for high-speed and low-power applications. Thefuture scope of this research lies in exploring novel designtechniques, power optimization, scalability, integration withadvanced process technologies, and real-world applications.By continuing toadvance thearea-effective and reduceddelay techniques, researchers can contribute to the evolutionofdigitalcircuits,leadingtomoreefficientandhigh-performancecomputingarchitectures.

Adderlogic	Cell delay(ns)	Total delay(ns)
Brent KungAdder	24.900	41.500
Ladner FischerAdder	23.600	42.400
PropagatorGeneratorAdder	20.600	34.100

Table 1.DelayComparison

TheaboveTable(1)tellsthedelaycomparisonofexistingandproposedadder.

VI. CONCLUSION

In conclusion, the design and implementation of anarea-effectiveandreduceddelaythree-operandparallelprefix adder offer significant benefits in terms of optimizinghardwareresourcesandimprovingcomputationalspeed.Through the application of area-effective techniques, suchas resource sharing and compact circuit layouts, the addercanutilize availablesilicon area efficiently. Additionally,the incorporation of delay reduction techniques, includingpropagationdelayoptimizationandgate-leveloptimizations,

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